TSMC-02-622

February 11, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

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Subject: | Serial No. 10/718,877 11/21/03 |

Shih-Wei Wang et al.

ENDURANCE IMPROVEMENT BY SIDEWALL NITRIDATION OF POLY FLOATING GATE FOR NONVOLATILE MEMORY DEVICES USING SUBSTRATE OR DRAIN-SIDE ERASE SCHEME

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B Ackerman 2/12/04

U.S. Patent 6,417,046 to Ho et al., "Modified Nitride Spacer for Solving Charge Retention Issue in Floating Gate Memory Cell," discloses a modified nitride spacer with significantly improved charge retention in floating gate memory cells.

U.S. Patent 6,184,088 to Kurooka et al., "Method for Manufacturing a Split Gate Type Transistor," teaches a method to fabricate a split-gate type transistor with a nitrated floating gate.

U.S. Patent 6,268,624 to Sobek et al., "Method for Inhibiting Tunnel Oxide Growth at the Edges of a Floating Gate during Semiconductor Device Process," discloses a method for inhibiting tunnel oxide thickening by forming protective barrier films.

U.S. Patent 5,966,606 to Ono, "Method for Manufacturing a MOSFET having a Side-wall Film Formed through Nitridation of the Gate Electrode," discloses a method for forming a sidewall film of a gate electrode by forming a thin silicon nitride film through nitridation of the gate electrode and a relatively thick silicon nitride film.

U.S. Patent 5,827,769 to Aminzadeh et al., "Method for Fabricating a Transistor with Increased Hot Carrier Resistance by Nitridizing and Annealing the Sidewall Oxide of the Gate Electrode," discloses a method for fabricating a transistor by nitridizing the sidewall oxide of the gate electrode.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-02-622	10/718,877
Applicant: Shih-Wei Wang et al.	
Filing Date: 11/21/03	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6417046	7/9/02	Ho et al.	438	257	5/5/00
	6184088	2/6/01	Kurooka et al.	438	264	2/25/99
	6268624	7/31/01	Sobek et al.	257	321	7/31/99
	5966606	10/12/99	Ono	438	303	5/14/97
	5827769	10/27/98	Aminzadeh et al.	438	305	11/20/96

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant